FINAL Reliability Report

STripFET™ F7 (OFT) Technology Front and Back Metal Capacity Extension - CT8" / SG8" Assembled in Shenzhen (China) INDUSTRIAL

General Information	
Product Lines:	OS43 – OL4P- OC43
P/N:	STL110N4F7HT (OS43) STL117N4LF7HT (OL4P) STL105N4LF7HT (OC43)
Product Group:	ADG
Product division:	Power Transistor Division
Package:	PowerFLAT™ 5x6
Silicon Process techn.:	Power MOSFET

Locations	
Wafer Fab and EWS Plant:	*CT8" (Italy)* *SG8" (Singapore)*
Assembly and testing plant:	*Shenzhen (China)*
Reliability Lab:	*ADG - Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	April 2017	8	A. Settinieri	C. Cappello	First issue

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify the new process on STripFET™ F7 (OFT) Front Wettable and Back Metal (Ti/Ni/Ag) manufactured in Ang Mo Kio SG8" (Singapore) – Assembled in Shenzhen (China)

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Power MOSFET

4.2 Construction note

D.U.T.: STL110N4F7HT PACKAGE: PowerFLAT™ 5x6

Wafer/Die Information	
Technology	Power MOSFET STripFET™ F7
Wafer Fab	CT8" (Italy)
Die finishing back side	Ti(0.7kA)/NiV(3kA)/Ag(1.5kA) @ SG8" (Singapore)
Die size	1430 x 2800 µm^2
Metal	AlCu
Passivation type	TEOS (5kA)/SiN (5.5kA)

Assembly/Testing information	
Assembly site	ST Shenzhen (China)
Package description	PowerFLAT™ 5x6
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Solder Paste Pb-Sn-Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Au Source: Clip
Lead finishing/bump solder material	Pure Tin

D.U.T.: STL117N4LF7HT PACKAGE: PowerFLAT™ 5x6

Wafer/Die Information	
Technology	Power MOSFET STripFET™ F7
Wafer Fab	CT8" (Italy)
Die finishing back side	Ti(0.7kA)/NiV(3kA)/Ag(1.5kA) @ SG8" (Singapore)
Die size	1710 x 2800 µm^2
Metal	AlCu
Passivation type	TEOS (5kA)/SiN (5.5kA)

Assembly/Testing information	
Assembly site	ST Shenzhen (China)
Package description	PowerFLAT™ 5x6
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Solder Paste Pb-Sn-Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Au Source: Clip
Lead finishing/bump solder material	Pure Tin

D.U.T.: STL105N4LF7HT PACKAGE: PowerFLAT™ 5x6

Wafer/Die Information	
Technology	Power MOSFET STripFET™ F7
Wafer Fab	CT8" (Italy)
Die finishing back side	Ti(0.7kA)/NiV(3kA)/Ag(1.5kA) @ SG8" (Singapore)
Die size	1640 x 2330 μm^2
Metal	AlCu
Passivation type	TEOS (5kA)/SiN (5.5kA)

Assembly/Testing information	
Assembly site	ST Shenzhen (China)
Package description	PowerFLAT™ 5x6
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Solder Paste Pb-Sn-Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Au Source: Clip
Lead finishing/bump solder material	Pure Tin

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot	Part Number	Silicon Lines	Wafer Fab	Front-Back metal process	Assy Plant	Comments
1	STL110N4F7HT	OS43	*CT8" (Italy)*	*SG8" (Singapore)*	Shenzhen *(China)*	
2	STL117N4LF7HT	OL4P				
3	STL105N4LF7HT	OC43				

5.2 Reliability test plan summary

#	Stress (Abrv)	PC	Std ref.	Conditions	Sample Size (S.S.)	Steps	Failure/SS		
							Lot 1	Lot 2	Lot 3
1	**TEST**		User specification	All qualification parts tested per the requirements of the appropriate device specification.			0/462	0/462	0/462
2	**External visual**		JESD22 B-101	All devices submitted for testing			0/462	0/462	0/462
3	**Pre-conditioning**		JESD22 A-113	Dryng 24H @ 125°C Store 168H @ TA=85°C,RH=85% IR Reflow @ 260°C 3 times		All devices to be subjected to H3TRB, TC, AC, IOL	0/308	0/308	0/308
4	**HTRB**	N	JESD22 A-108	Tj = 175°C ; BIAS = 32V	362	1000h	0/45	0/45	0/45
5	**HTGB**	N	JESD22 A-108	TA=175°C ; BIAS= 20V	231	1000H	0/45	0/45	0/45
6	**TC**	Y	JESD22 A-104	TA=-65°C TO 150°C 1 HOURS / CYCLE	308	500cy	0/25	0/25	0/25
7	**AC**	Y	JESD22 A-102	TA=121°C ; PA=2ATM	358	96H	0/25	0/25	0/25
8	**H3TRB**	Y	JESD22 A-101	TA=85°C ; RH=85% BIAS=32V	358	1000H	0/25	0/25	0/25
9	**IOL**	Y	MIL-STD-750 Method 1037	ΔTj ≥100°C	308	15Kcy	0/25	0/25	0/25
10	**ESD**		AEC Q101-001,002 and 005	CDM / HBM	9		0/3	0/3	0/3

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB / HTFB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
IOL / TF Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB/THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Dear Customer,

Following the continuous improvement of our service and in order to increase productivity, this document is announcing that Wafer Front (Wettable)/Back Metal Finishing process and EWS (Wafer Testing) for STripFET™ F7 (OFT) technology currently manufactured in Catania and in our Subcontractor HHGrace will be also done in ST's Ang Mo Kio (Singapore) FAB.

Manufacturing process between Catania, HHGrace and Ang Mo Kio are very similar thus wafers produced in Ang Mo Kio (Singapore) FAB, guarantees the same quality and electrical characteristics as per current production.

The involved product series and affected packages are listed in the table below:

Product Family	Technology	Part Number
Power MOSFET Transistors	STripFET™ F7	See involved product list

Any other Product related to the above series, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from **week 30-2017**.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Part Number - Test Vehicle
Power MOSFET Transistors	PowerFLAT™ 5x6	STL110N4F7HT STL117N4LF7HT STL105N4LF7HT

Change implementation schedule:

The production start and first shipments will be implemented after week 30 of 2017.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of STripFET™ F7 (OFT) technology manufactured in ST's Ang Mo Kio (Singapore) FAB, will be ensured by internal code (Finished Good) and Q.A. number.

Yours faithfully.

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : STripFET™ F7 (OFT) Technology Front and Back Metal Capacity Extension - Ang Mo Kio (Singapore)
PCN Reference : ADG/17/10232

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STL220N6F7	STL130N6F7	STL90N6F7
STL20N6F7	STL120N8F7	STL140N6F7
STL100N8F7	STL110N10F7	STL130N8F7

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